3. STATUS OF THE CLAIMS

Claims 36-39, 59-69, and 75-83 are currently pending and are appealed. No claims have been canceled or added. The pending claims are listed in Appendix I.

4. STATUS OF AMENDMENTS

No amendments have been made subsequent to the Office Action mailed on August 9, 2002.

5. SUMMARY OF THE INVENTION

As described in the Appellants' specification at page 7, line 6 - page 8, line 13, and shown generally in figures 9-11, embodiments of the invention disclosed relate to a memory device that selectably operates using both burst and pipelined modes of operation. In one embodiment, an asynchronously addressable storage device 100 (shown in FIG. 9) includes mode circuitry 121 configured to select between burst and pipelined modes, and circuitry 122 operable in either the burst mode or pipelined mode and configured to switch between the burst mode and the pipelined mode for operating the device 100 in either mode. (Pg. 29, lines 5-25). Some embodiments can switch between burst access and ... pipelined modes of operation without ceasing ("on the fly"). (Pg. 33, lines 17-19). In the burst mode of operation, an externally-generated memory address stored in the circuitry 122 is first used to select data within the device 100. A counter 149 included in the circuitry 122 then increments the stored external address to internally generate addresses for subsequent accesses. In the pipelined mode of operation, the circuitry 122 uses external addresses 115 to access data within the device 100. (Pg. 29, lines 8-16). As address information passes through the memory, it is operative in one operational area before moving into another operational area. However, once moved, another set of address information may enter the operational area exited, and accesses to memory may overlap without conflicting. (Pg. 8, lines 1-5). In addition to the embodiments described, the invention includes other embodiments of varying scope, including systems, methods, and storage devices, such as memory circuits. (Pg. 33, line 23 - Pg. 40, line 19).

6. ISSUES PRESENTED FOR REVIEW

1. Whether claims 36-39, 59-64, 69, and 75-83 were properly rejected under 35 USC § 102(e) as being anticipated by U.S. Patent No. 5,610,864, issued to Manning, hereinafter "Manning".

2. Whether claims 65-68 were properly rejected under 35 USC § 103(a) as being unpatentable over Manning in view of U.S. Patent No. 5,587,964, issued to Rosich et al., hereinafter "Rosich".

7. GROUPING OF THE CLAIMS

All claims are to be taken independent of each other and each stands alone for purposes of this appeal.

8. ARGUMENT

a) The Applicable Law

Anticipation requires the disclosure in a single prior art reference of each element of the claim under consideration. *In re Dillon* 919 F.2d 688, 16 USPQ 2d 1897, 1908 (Fed. Cir. 1990) (en banc), cert. denied, 500 U.S. 904 (1991). It is not enough, however, that the prior art reference discloses all the claimed elements in isolation. Rather, "[a]nticipation requires the presence in a single prior reference disclosure of each and every element of the claimed invention, *arranged as in the claim.*" *Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co.*, 730 F.2d 1452, 221 USPQ 481, 485 (Fed. Cir. 1984) (citing *Connell v. Sears, Roebuck & Co.*, 722 F.2d 1542, 220 USPQ 193 (Fed. Cir. 1983)) (emphasis added). "The identical invention must be shown in as complete detail as is contained in the ... claim." *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989); MPEP § 2131.

The Examiner has the burden under 35 U.S.C. § 103 to establish a *prima facie* case of obviousness. *In re Fine*, 837 F.2d 1071, 1074, 5 U.S.P.Q.2d (BNA) 1596, 1598 (Fed. Cir. 1988). In combining prior art references to construct a *prima facie* case, the Examiner must show some

objective teaching in the prior art or some knowledge generally available to one of ordinary skill

in the art that would lead an individual to combine the relevant teaching of the references. *Id.*

The M.P.E.P. contains explicit direction to the Examiner that agrees with the *In re Fine* court:

> In order for the Examiner to establish a *prima facie* case of obviousness, three base
>
> criteria must be met. First, there must be some suggestion or motivation, either in
>
> the references themselves or in the knowledge generally available to one of ordinary
>
> skill in the art, to modify the reference or to combine reference teachings. Second,
>
> there must be a reasonable expectation of success. Finally, the prior art reference (or
>
> references when combined) must teach or suggest all the claim limitations. The
>
> teaching or suggestion to make the claimed combination and the reasonable
>
> expectation of success must both be found in the prior art, and not based on
>
> applicant's disclosure. *M.P.E.P.* § 2142 (citing *In re Vaeck*, 947 F.2d 488, 20
>
> U.S.P.Q.2d (BNA) 1438 (Fed. Cir. 1991)).

An invention can be obvious even though the suggestion to combine prior art teachings is

not found in a specific reference. *In re Oetiker*, 977 F.2d 1443, 24 U.S.P.Q.2d (BNA) 1443 (Fed.

Cir. 1992). However, while it is not necessary that the cited references or prior art specifically

suggest making the combination, there must be some teaching somewhere which provides the

suggestion or motivation to combine prior art teachings and applies that combination to solve the

same or similar problem which the claimed invention addresses. One of ordinary skill in the art

will be presumed to know of any such teaching. (See, e.g., *In re Nilssen*, 851 F.2d 1401, 1403, 7

U.S.P.Q.2d 1500, 1502 (Fed. Cir. 1988) and *In re Wood*, 599 F.2d 1032, 1037, 202 U.S.P.Q.

171, 174 (C.C.P.A. 1979)). However, the level of skill is not that of the person who is an

innovator but rather that of the person who follows the conventional wisdom in the art. *Standard*

Oil Co. v. American Cyanamid Co., 774 F.2d 448, 474, 227 U.S.P.Q. 293, 298 (Fed. Cir. 1985).

The requirement of a suggestion or motivation to combine references in a *prima facie* case of

obviousness is emphasized in the Federal Circuit opinion, *In re Sang Su Lee*, 277 F.3d 1338; 61

U.S.P.Q.2D 1430 (Fed. Cir. 2002), which indicates that the motivation must be supported by

evidence in the record.

The test for obviousness under § 103 must take into consideration the invention as a whole; that is, one must consider the particular problem solved by the combination of elements that define the invention. *Interconnect Planning Corp. v. Feil*, 774 F.2d 1132, 1143, 227 U.S.P.Q. 543, 551 (Fed. Cir. 1985). The Examiner can only rely on references which are either in the same field as that of the invention, or if not in the same field, the references must be "reasonably pertinent to the particular problem with which the inventor was concerned." *M.P.E.P.* § 2141.01 (a) (citing *In re Oetiker*, 24 U.S.P.Q.2d (BNA) 1443 at 1445). The Examiner must also recognize and consider not only the similarities but also the critical differences between the claimed invention and the prior art. *In re Bond*, 910 F.2d 831, 834, 15 U.S.P.Q.2d (BNA) 1566, 1568 (Fed. Cir. 1990), *reh'g denied*, 1990 U.S. App. LEXIS 19971 (Fed. Cir. 1990).

If the proposed modification renders the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification. *M.P.E.P.* § 2143.01 (citing *In re Gordon*, 733 F.2d 900, 221 U.S.P.Q. 1125 (Fed. Cir. 1984)). The Examiner must also avoid hindsight. *Id.* The Examiner cannot use the Appellant's structure as a "template" and simply select elements from the references to reconstruct the claimed invention. *In re Gorman,* 933 F.2d 982, 987, 18 U.S.P.Q.2d (BNA) 1885, 1888 (Fed. Cir. 1991).

b) The References

Manning: teaches a memory device which can be accessed using latched row and column addresses. (Col. 4, lines 10-28). The device may also be accessed using a high-speed burst mode of operation, wherein the address is incremented internal to the device, using transitions of the column address select (/CAS) signal, following the assertion of a single external column address. (Col. 4, lines 29-49). Switching between the burst extended data out (EDO) mode and the standard EDO mode is described. (Col. 6, lines 14-22). Switching between interleaved and linear addressing modes is mentioned. (Col. 6, lines 30-34). The possibility of applying a pipelined architecture to Manning's invention is also mentioned. (Col. 5, lines 43-46). Operation of the pipelined architecture is said to be characterized by having a memory

throughput of less than one access per cycle, such that the data coming out of the device is offset by some number of cycles equal to the pipeline length. (Col. 5, lines 46-50). However, no details of how to apply the architecture, or its operation, are given.

Rosich: describes a dynamic random access memory (DRAM) device which uses the state of the write enable (WE) signal to select page mode or nibble mode operation at the first column address strobe (CAS) signal assertion after a row address strobe (RAS) signal assertion. (Col. 6, lines 25-28). After being placed in nibble mode, the counter enable (CEN) signal permits a counter to internally increment column addresses. (Col. 7, lines 18-21; and FIG. 5A). Pipelined operation is not discussed.

c) Discussion of the Rejections

c.1 The rejection under § 102:

Claims 36-39, 59-64, 69, and 75-83 were rejected under 35 USC § 102(e) as being anticipated by Manning. First, the Appellants do not admit that Manning is prior art and reserve the right to swear behind this reference in the future. Second, the Appellants respectfully submit that a case of anticipation under 35 U.S.C. § 102(e) has not been established because Manning does not disclose each and every element of claims 36-39, 59-64, 69, and 75-83. Therefore, the Appellants respectfully traverse this rejection under 35 U.S.C. § 102(e).

Why the reference does not disclose each and every element of the claimed subject matter as arranged in the claims.

Manning specifically fails to disclose "selecting between a burst mode and a pipelined mode of operation" as claimed by the Appellants in claims 36, 63, and 68. Similarly, Manning fails to disclose the order of address access "in the pipelined mode" (claims 37, 76, and 81), or "in the burst mode" in conjunction with selecting between the burst and pipelined modes of operation (claim 38); or "selecting at least one address pathway based on the selection between the burst mode and the pipelined mode" (claim 39).

Further, Manning fails to teach "choosing whether the memory is in a burst mode ... or in a pipeline mode of operation", "switching between the burst mode ... and the pipelined mode", "switching between ... read ... and write operation[s]" in conjunction with choosing a pipelined

mode of operation, or "operations ... performed in a different order" in conjunction with choosing a pipelined mode of operation (claims 59-62).

In addition, Manning fails to describe "selecting an external address only data path ... if ... the pipelined mode of operation is selected" (claims 63 and 68), and "operations ... performed in a different order" (including selecting a pipelined mode of operation) (claim 64). Manning also fails to describe "changing [a] ... mode select signal to select a pipelined mode of operation" (claims 65 and 67), and "switching the mode of operation to a pipelined mode" (claim 66).

Finally, Manning fails to include any teaching of "switching from a burst mode ... to a pipelined mode" (claims 75 and 80), "selecting at least one address pathway" based upon such switching (claims 77 and 82), "subsequently switching from the pipelined mode ... to the burst mode" (claims 78 and 83), or "selecting at least one address pathway" based upon such subsequent switching (claim 79). Manning also fails to describe a storage device including mode circuitry "configured to select between a burst mode and a pipeline mode" along with "an external column address data path for pipeline read and write operation column address generation" (claim 69).

Several assertions were made in the Office Action which attribute support to various concepts allegedly disclosed by Manning. However, a careful reading of each citation reveals that the discussion of the asserted elements is erroneous. These assertions have been made with respect to:

Claim 36, 60, 75, and 80 - Manning does not disclose switching or selecting between a burst mode and a pipelined mode (Manning never discusses switching or selecting between the modes, only operation in the burst mode, and the possibility of using a pipelined architecture).

Claims 37, 76, and 81 - Manning does not disclose obtaining a second external column address ... for operation in the pipeline mode (Manning merely refers to the possibility of using a pipelined *architecture*, and never discusses the details of how it might operate).

Claim 39, 77, 82 - Manning does not disclose selecting an address pathway based on ... selection between a burst mode and a pipelined mode (since Manning never discloses selecting between burst and pipelined modes in the same device).

Claims 78, 79, and 83 - Manning does not disclose, discuss, or teach switching from pipelined mode to burst mode (Manning merely refers to the possibility of using a pipelined *architecture*).

Claims 63 and 69 - Manning does not disclose an external address only path for the pipeline mode, or pipeline/burst circuitry (since Manning explains nothing about a pipelined architecture, other than generally characterizing its operation).

Why the reference does not disclose the claimed subject matter in as complete detail as is contained in the claim.

First, it should be noted that the Office has admitted that "Manning does not specifically disclose a mode select pin and a mode control signal for selecting between a burst and a pipeline mode of operation." in an Office Action mailed to the Appellants on July 18, 2001 (Application Ser. No. 08/984,701, Paper 19, page 7) with regard to similar subject matter. If Manning does not disclose these elements, how (specifically) does Manning support *switching* or *selecting* between burst and pipelined modes of operation, as claimed in claims 36, 59, 63, 65, 66, 67, 68, 69, 75, and 80 (and in all claims that depend from them)?

Second, the Office has failed to establish a case of anticipation. While the assertion is made that Manning discloses "choosing whether the memory is in burst or a pipelined mode of operation","switching between a burst mode and a pipeline mode", and "pipeline/burst circuitry", the Appellants' representative, after a careful study of Manning, was unable to locate any such discussion, nor any such circuitry which was configurable to select or switch between burst and pipelined modes of operation.

For example, the only elements offered by the Office to support the assertion that Manning "discloses the invention as claimed" with respect to claims 36, 75, and 80 are: FIG.1 EDO signal, and FIG. 2 ADDR, ROW, COLm, and /WE signals; col. 5, lines 41-50; col. 6, lines 14-34; and col 7, lines 43-54. Fig. 1 is a block diagram of an EDO memory that operates in burst or page modes, with no indication regarding exactly which modes may be operative, or how they may be selected. Col. 5, lines 41-50 discuss the possibility of using a pipelined architecture, but not as enabling switching between pipeline mode and burst operations within the *same* memory, as disclosed and claimed by the Appellants. Col. 6, lines 14-34 merely describe burst and

"standard" (i.e., page mode - see col. 6, lines 18-19) EDO operations. Finally, col. 7, lines 43-54 speak to switching between non-EDO and EDO page modes, a static column mode, and a burst mode. Thus, Manning never discusses the ability to *select* or *switch* between burst and pipelined modes of operation, or circuitry to effect such a selection, as claimed by the Appellants in independent claims 36, 59, 63, 65, 66, 67, 68, 69, 75, and 80, and all of the claims which depend from them. It should also be noted that one does not have to "select pipeline mode" to "work in the pipeline architecture," as asserted in the Office Action. For example, if a device always operates in the pipelined mode, and is unable to switch to another mode, the pipelined mode does not have to be selected.

Another way of viewing this issue is to ask the question: How can a memory have a pipelined architecture (as mentioned by Manning) without inherently operating in the pipelined mode (as claimed by the Appellants)? The brief answer is that a memory, such as a burst EDO memory, may include pipelined registers that permit the rapid generation of *internal* addresses. However, *external* addresses are still received and processed in the same fashion as regular EDO memory. See, for example, the definition for "Burst Extended Data Output RAM (BEDO)", Shuttle Inc., Frequently Asked Questions, December 14, 1999, attached hereto as Appendix II.

In memory terminology, a row of memory cells is called a page. With page-mode memory, a row address is applied to the chip and the RAS signal held active while sequential column addresses are applied and the CAS signal cycled until an entire row of memory cells are read or written. By addressing columns in this manner, all of the memory cells in a selected row can be written or read without changing the row address. Since page-mode memory requires a setup time for each column address, it was eventually replaced with fast page-mode memory.

Fast page-mode memory eliminates most of the setup time for column addresses within a page, so it is faster and consumes less power than page-mode memory. With fast page-mode memory, memory accesses for an entire page were usually fast enough to reduce wait states in processors available for use with this type of memory. However, when the processor requests data from a different page, both row and column addresses have to be changed, and the resulting delay is similar to ordinary page-mode operation. See "Fast Page Mode (FPM)", Id.

EDO memory is similar to fast page-mode memory in that an entire page of memory can be read very quickly. The major advantage of EDO memory is that it modifies CAS timing to hold data at the chip's output pins longer. This means that the output data can be read while the CAS signal is de-asserted and set up for the next cycle, resulting in less waiting. With EDO memory, data can be read or written (within a page) as fast as the memory chip will accept new column addresses. EDO allows more overlap between column accesses and data transfers than fast page-mode memory, eliminating most of the wait and resulting in a considerable performance improvement. See "Extended Data Output RAM (EDO)", Id.

Burst EDO memory improves EDO performance by adding **a pipeline stage** (i.e. **a pipelined architecture**) to permit reads or writes to occur in four row-address bursts. After the initial page address is applied to a burst EDO chip, the chip typically provides three more sequential addresses (within a page). This address circuitry eliminates the time required to detect and latch externally supplied addresses. However, burst EDO memory including a pipelined architecture does not accept external addresses so as to operate in a pipelined mode (as defined by the Appellants in the Application). See "Burst Extended Data Output RAM (BEDO)", Id.

In some embodiments of the Appellants' invention, a newburst signal from control logic is provided. The newburst signal is fed to a multiplexer for choosing which type of addressing is to occur. For one type of addressing, burst operation is provided beginning with a stored initial external address. A counter is then used to increment the initial external address. (Application, Pg. 29, lines 8-25)

In pipelined mode, address information is divided into operational times. As address information passes through the memory, it is operative in one operational area before moving onto another operational area. However, once moved, another set of address information may enter the operational area exited. Thus, by time slicing address information, accesses to a memory may overlap without conflicting. This allows for a continuous data stream of address information in the form of external addresses. Therefore, **internal addresses are not generated in pipelined mode**. Rather, addresses are provided from an external source as a stream of data. In page mode, with one enable signal held active and another enable signal cycled, an external address is received on each cycle of the cycled enable signal. For example, if /RAS is held

active, and /CAS is cycled, a random or determined order of columns associated with the row

address may be accessed in pipelined mode, whereas in burst mode, a predetermined pattern of

columns may be accessed. (Application, Pg. 8, lines 1-13)***

In short, what is discussed by Manning is not identical to the subject matter of the present

invention as required by the M.P.E.P., and therefore, the rejection under § 102 is improper.

Reconsideration and allowance of claims 36-39, 59-64, 69, and 75-83 is respectfully requested.

c.2 The rejection under § 103:

Claims 65-68 were rejected under 35 USC § 103(a) as being unpatentable over Manning

in view of Rosich. First, the Appellants do not admit that Manning or Rosich are prior art and

reserve the right to swear behind these references in the future. Second, since each of the

references fail to teach the element of *switching, selecting, or choosing* between pipelined and

burst modes of operation, since the proposed combination of references would be inoperative,

and since the references teach away from such a combination, the Appellants respectfully

traverse this rejection under § 103 by the Office.

The Appellants are unable to find how combining Manning with Rosich serves to teach

the invention disclosed in claims 65-68. The Appellants have already discussed why Manning is

defective as a reference (i.e., Manning does not disclose *selecting, choosing, or switching*

between burst and pipelined modes of operation). Even so, many assertions are made in various

Office Actions respecting the instant Application to the effect that Manning discloses switching

or changing modes to a pipelined mode (even to the extent of specifying where in the cycles of a

memory operation the change to a pipelined mode occurs (see § 9 of the Office Action mailed to

the Appellants on 3/15/02, regarding claims 66-67). However, the Appellants can find no such

teaching in Manning. No reply has been received by the Appellants in response to several

requests for more specific citations to how such activity is enabled by the references. Instead the

single statement in Manning (col. 5, lines 43-50) which alludes to the possible existence of a

pipelined architecture has been repeatedly presented by the Office. This text provides no

description as to how the architecture would be implemented, especially with regard to changing

between a pipelined mode and other operational modes at will, in the same memory, using

individual operational signals, as occurs in some of the embodiments disclosed by the

Appellants. As explained above, this is because the term "pipelined architecture" refers to

pipelined registers used for the rapid generation of *internal* addresses in burst EDO memory.

In rejecting claim 65, the Office Action states: "Rosich discloses the step of changing the

mode select signal to select a mode of operation while maintaining a first enabling signal in an

active state ... (... RASL in Fig. 7)". From this statement, it is apparent that the RAS L signal of

Rosich is being interpreted in the Office Action as the "first enabling signal" of claim 65. Thus,

the Office Action relies on Rosich to teach switching modes of operation while maintaining the

RAS L signal in the active state. However, it should be noted that Rosich specifically states "...

the DRAM **will not change from page mode to nibble mode** until the next assertion of the

CAS signal after the assertion of the RAS signal." See Rosich et al., Col. 9, lines 6-9. In other

words, until the RAS signal as been re-asserted (not "maintained", as claimed by the Appellants),

changing operational modes is not possible.

Further support for this operational requirement of the device disclosed by Rosich can be

found by referring to FIG. 5A of Rosich. If WE L is not asserted (i.e., is high, indicating a read)

on the first assertion of CAS L following the assertion of RAS L, the counter enable (CEN)

signal will be high, and the DRAM will be configured for nibble mode. If, on the other hand,

WE L is asserted (i.e., is low, indicating a write) on the first assertion of CAS L following an

assertion of RAS L, CEN will be low, and the DRAM will be configured for page mode. In

either case, after the DRAM configuration has been selected following assertion of the RAS L

signal, the configuration cannot be switched until after the RAS L signal is deasserted (clearing

flip-flops 540 and 550 in FIG. 5A). This is consistent with the specification in Rosich, which

states "The DRAM will **remain in nibble mode until RAS is deasserted** resetting the outputs of

flip-flop 550". See Rosich et al., Col. 8 lines 49-50. Thus, once the DRAM is configured for

either the nibble mode or page mode following an assertion of RAS L, the DRAM will *remain in*

that mode until after the RAS L signal is deasserted and then asserted again.

Therefore, the Office Action assertion that Rosich discloses switching modes of operation

while maintaining the RAS L signal in active state is erroneous, and it is respectfully submitted

that the Office Action has failed to make out a *prima facie* case of obviousness at least because

the cited references do not show or suggest "changing the mode select signal to select a pipeline mode while maintaining a first enabling signal in an active state", as recited in claim 65.

Rosich merely discloses switching between a page mode and a nibble mode. There is no discussion of a pipelined access mode by Rosich, whatsoever. Thus, the combination of Rosich with Manning does not cure the admitted primary defect of Manning, nor the failure of each of the cited references to disclose switching between burst and pipelined modes of operation.

The assertion has been made in the Office Action that "one of ordinary skill in the art ... would have recognized that the memory access cycle of Manning would have been reduced by maintaining a first enable signal in an active state during mode [sic] of operations because it would provide a capability of that the memory is always in ready [sic] to receive a mode command thereby increasing the access speed of the memory. Increasing memory speed would have a highly desirable feature in the computer system environment of Rosich because the objective of computer system [sic] is increasing speed or computing power. Therefore, it would have been obvious to incorporate the step of maintaining a first enabling signal in [sic] active state of Rosich in Manning because it would increase memory access speed of Manning by providing a capability of that the memory is always in [sic] ready to receive a command." However, as demonstrated above, maintaining the state of the RAS L signal *prohibits* changing modes. Thus, there is no evidence in the record as to why it would be obvious to incorporate Rosich's RAS L signal into the operation of Manning to provide *a single memory device which selectably operates in both burst and pipelined modes*, as occurs in some embodiments disclosed by the Appellants. This complete absence of evidence in the record fails to satisfy the explicit requirements set forth by the *In re Sang Su Lee* court. Thus, the Examiner appears to be using personal knowledge to support this combination of references, and is respectfully requested to submit an affidavit as required by 37 C.F.R. § 1.104(d)(2).

Finally, Rosich teaches away from the combination urged by the Office Action because, as has already been demonstrated, Rosich's RAS L signal *can not* be maintained while mode changes are effected. The M.P.E.P. requires that any asserted combination of references must not render the prior art unsatisfactory for its intended purpose, or change the principle of operation of the reference being modified. *See* M.P.E.P. § 2143.01. One of ordinary skill in the art would not

be led to change modes in the device of Manning by using an inoperable mechanism of Rosich. Such modification would render the apparatus of Manning unfit for its intended purpose.

Since the page/nibble mode DRAM of Rosich, as well as the EDO memory of Manning do not include each of the elements claimed by the Appellants, since there is no evidence in the record supporting a motivation to combine the references, and finally, since the references teach away from such a combination, the Appellants respectfully request reconsideration and withdrawal of the rejection of claims 65-68 under 35 U.S.C. §103.

c.3 Why the claims are separately patentable:

Independent claim 36 includes "selecting between a burst mode and a pipelined mode of operation of ... [an] asynchronously accessible DRAM". Dependent claims 37-39 refine this concept by including the limitations on the order of address access "in the pipelined mode" (claims 37), or "in the burst mode" in conjunction with selecting between the burst and pipelined modes of operation (claim 38); and "selecting at least one address pathway based on the selection between the burst mode and the pipelined mode" (claim 39). None of these limitations depends on the other, and each dependent claim is separately patentable from the other, and from independent claim 36.

Independent claim 59 includes the element of "choosing whether the memory is in a burst mode ... or in a pipeline mode of operation". Dependent claims 59-62 add the limitations of "switching between the burst mode ... and the pipelined mode", "switching between ... read ... and write operation[s]" in conjunction with choosing a pipelined mode of operation, and "operations ... performed in a different order" in conjunction with choosing a pipelined mode of operation. None of these limitations depends on the other, and each dependent claim is separately patentable from the other, and from independent claim 59.

Independent claims 63 and 68 include "selecting an external address only data path ... if ... the pipelined mode of operation is selected". Dependent claim 64 adds the further limitation of "operations ... performed in a different order" (including selecting a pipelined mode of operation), while independent claim 63 adds the further limitation of "receiving an external row address". None of these limitations depends on the other, and each dependent claim is separately patentable from the other, as well as from the independent claims.

Independent claim 65 and 67 include "changing [a] ... mode select signal to select a pipelined mode of operation", while dependent claim 66 adds the limitation of "switching the mode of operation to a pipelined mode". Independent claim 65 includes the additional limitation of "receiving a mode select signal". None of these limitations depends on the other, and each dependent claim is separately patentable from the other.

Independent claim 69 describes a storage device including mode circuitry "configured to select between a burst mode and a pipeline mode" along with "an external column address data path for pipeline read and write operation column address generation". This independent apparatus claim is separately patentable from all of the other claims.

Independent method claims 75 and 80 include the element of "switching from a burst mode ... to a pipelined mode", while dependent claims 77 and 82 add the limitation of "selecting at least one address pathway" based upon such switching. Dependent claims 78 and 83 add the limitation of "subsequently switching from the pipelined mode ... to the burst mode", while dependent claim 79 adds the limitation of "selecting at least one address pathway" based upon such subsequent switching. Independent claim 75 adds the possiblity of "selecting a ... write operation." None of these limitations depends on the other, and each dependent claim is separately patentable from the other, as well as from the independent claims.

c.4 Double patenting rejection:

Claim 66 was provisionally rejected under the judicially created doctrine of double patenting over claims 51, 59, 63, 64, and 67 of co-pending Application No. 08/984,561. Since co-pending U.S. Patent Application Serial No. 08/984,561 has not yet received any final indication of allowed claims, the Appellants request that the claims of the instant Application be allowed to issue without a Terminal Disclaimer, and that the issued claims of the instant Application be compared to the claims of the cited co-pending application to determine if a judicially-created non-statutory double patenting rejection is required. If so, the Appellants will submit a Terminal Disclaimer to obviate any remaining double patenting rejections upon closing prosecution on the merits for the co-pending application, as needed, or in the alternative, upon receiving an indication of allowance for the relevant claims in the instant Application.

9. SUMMARY

It is respectfully submitted that the art cited does not anticipate the claimed invention, nor does the cited art render the claimed invention obvious. It is respectfully submitted that claims 36-39, 59-69, and 75-83 should therefore be allowed. Reconsideration and withdrawal of the rejections of claims 36-39, 59-69, and 75-83 is respectfully requested. Should the Board be of the opinion that a rejected claim may be allowable in amended form, an explicit statement to that effect is also respectfully requested.

CONCLUSION

The Appellants respectfully submit that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Appellants' attorney, Mark Muller, at (210) 308-5677, or the undersigned attorney, to facilitate prosecution of this application. If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.
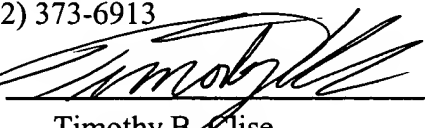
Respectfully submitted,

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Date 12 Nov. 2002   By _____

Timothy B. Clise
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